REMARKS

Claims 1-35 are pending in the present application. By this amendment, claims 1-5, 20-22, 24-25, 27, 29-31, and 33-34 have been amended, and claims 36-47 have been added. No new matter has been added. Accordingly, claims 1-47 are currently under consideration. Applicants respectfully submit that these claims are allowable.

Objections to Specification

The specification stands objected to because of certain informalities. Appropriate amendments have been made. No new matter has been added. Applicants respectfully request that the above-cited objection be withdrawn.

Claim Rejections Under 35 USC § 112

Claims 1-8 stand rejected under 35 U.S.C § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicants regard as the invention. Claims 1 and 3 have been amended to clarify the language of the claims.

Applicants respectfully request that the above-cited rejection under 35 U.S.C § 112, second paragraph, be withdrawn.

Claim Rejections Under 35 USC § 102 and 35 USC § 103

Claims 1, 5, 6, 7, 20, and 23 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Agrawal et al. (U.S. Patent No. 5,490,074, hereinafter Agrawal). Claims 2, 3, 9-17, 21, and 22 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Agrawal in view of Young (U.S. Patent No. 5,818,730, hereinafter Young). Applicants respectfully submit that the claims, as amended, are allowable over the cited references and all references of record.

Claim 1, as amended, defines *"a routing architecture" "wherein the wires oriented in the first direction have a physical length that is substantially the same as an electrically optimum*

physical length or an adjustment of the electrically optimum physical length to account for non-electrical considerations." According to the Office Action, "Young is cited primarily to show that routing efficiency and utilization of wires having electrically optimum physical lengths would have been obvious features to implement in a PLD." However, the Examiner has improperly conflated "routing efficiency" with "*the electrically optimum physical length.*"

"Routing efficiency" is generally understood to mean the efficiency, in terms of the overall area on a silicon chip, to implement a given amount of routing. In general, there are three primary aspects to this (considered alone or in combination). The first is the actual amount of silicon area required to construct a routing wire of a given type, where this area should be minimized. The second is the pattern, or more specifically the topology or arrangement of connections from routing wires to other routing wires, which should be chosen to maximize the number of different combinations of routing wires that can be used to provide a particular routing connection on the chip, in order to be able to use each wire with a high probability. The third is the length of each wire, which should be chosen with regard to the length of typical connections on the die. As the length of routing wires increases, the cost also increases, so there tends to be a length that implements typical connections most efficiently. In general, electrical optimality (i.e., speed optimality) of long distance connections is not a design goal in routing efficiency.

The Young patent discusses relevant design goals at column 1, lines 38-52:

> "To minimize cost, surface area must be used efficiently, particularly where a relatively large number of signal paths must be provided within a relatively small diffusion area. ... A structure and method are provided for designing the wiring layout or routing paths in a programmable logic integrated circuit device for maximizing the number of paths for an available diffusion area, or alternatively, for minimizing the required diffusion area for a given number of paths."

Additionally, at column 5, lines 18-27, the Young patent specifically discusses design goals related to routing efficiency, here addressing the number of distinct paths. This section speaks to the topology of the routing connections and focuses on providing the largest number of distinct routing paths within the routing structure. While the Young patent does disclose a focus on routing efficiency, including the various aspects described above for minimizing the overall area on a silicon chip for a given amount of routing, this reference does not disclose electrical optimality as a design goal (e.g., to maximize speed for long distance connections). Neither Young nor Agarwal disclose this consideration as a design goal. By contrast, the disclosure of the present invention teaches electrical optimality (i.e., speed optimality) as a design goal. (See for example, page 4, lines 5-7, of the present specification.)

The above-cited characteristic features of the present invention, defined clearly in claim 1 of the present invention, are not disclosed in the cited references. Therefore, claim 1 is allowable over the cited references. Because they depend directly or indirectly from claim 1, claims 2-8 are likewise allowable over the cited references.

Claim 9 defines *"a two-dimensional routing architecture"* including *"a wire having a logical length that is a function of an orientation of the wire and having a physical length that is substantially the same as an electrically optimum physical length or an adjustment of the electrically optimum physical length to account for non-electrical considerations."* For the reasons presented above with respect to claim 1, claim 9 is allowable over the cited references. Because they depend directly or indirectly from claim 9, claims 10-14 are likewise allowable over the cited references.

Claim 15 defines *"method to interconnect a plurality of function blocks within a programmable logic device"* including *"connecting the plurality of function blocks to the wire having a physical length that is substantially the same as the physical length that is electrically optimum."* For the reasons presented above with respect to claim 1, claim 15 is allowable over

the cited references. Because they depend directly or indirectly from claim 15, claims 16-19 are likewise allowable over the cited references.

Claim 20, as amended, defines *"a two-dimensional routing architecture"* where *"the physical length of the first subset of the plurality of wires is substantially the same as an electrically optimum physical length or an adjustment of the electrically optimum physical length to account for non-electrical considerations."* For the reasons presented above with respect to claim 1, claim 20 is allowable over the cited references. Because they depend directly or indirectly from claim 20, claims 21-23 are likewise allowable over the cited references.

Applicants respectfully request that the above-cited rejections under 35 U.S.C. § 102 and 35 U.S.C. § 103 be withdrawn.

Allowable Subject Matter

Claims 18 and 24-35 stand objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims.

Claim 24 has been rewritten accordingly in independent form. Therefore claim 24 is allowable. Because they depend directly or indirectly from claim 24, claims 25-35 are likewise allowable. Changes to these claims have been made to improve formal structure and not to overcome a rejection based on cited prior art. As discussed above, claim 18 is allowable because it depends from claim 15, which is allowable. Applicants respectfully request that the above-cited objection be withdrawn.

New Claims

Claims 36-47 have been added to the application. Applicants submit that these new claims are distinguishable over the cited references and all references of record.

CONCLUSION

All objections and rejections having been addressed, it is respectfully submitted that the present application is in condition for allowance and a Notice to that effect is earnestly solicited. If it is determined that a telephone conference would be helpful in advancing this case to an allowance, the Examiner is invited to contact the undersigned by telephone.

In the unlikely event that the transmittal letter is separated from this document and the Patent Office determines that an extension and/or other relief is required, applicants petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to Deposit Account No. 03-1952 referencing docket no. **306812002500**. However, the Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Respectfully submitted,

Dated: April 15, 2004 By: _____

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